# A high power density and high efficiency UHF-band HFET for low voltage operation

T. Kunii, Y. Kohno, T. Kitano, S. Miyakuni, J.Udomoto,
K. Yamamoto, K. Maemura, H.Takano, O. Ishihara, and N. Tsubouchi

Optoelectronic and Microwave Devices Laboratory, Mitsubishi Electric Corporation
4-1, Mizuhara, Itami, Hyogo 664, Japan
TEL:+81-727-84-7386, FAX:+81-727-80-2694, e-mail : kunii@oml.melco.co.jp

## Abstract

**A high power density and high efficiency AlGaAs/GaAs Heterostructure FET (HFET) for 0.9GHz Digital Cellular Phone Systems has been successfully developed. The device has delivered a high power density of 117mW/mm with a power-added efficiency (PAE) of 37.6% with a low adjacent channel power (ACP) of -53.4dBc at a low drain bias of 3.3V at 950MHz operating frequency.**

## Ⅰ. Introduction

Recently, low voltage operation devices with a high power and a high efficiency for Digital Cellular Phone Systems have been demonstrated [1][2]. These devices have larger total gate widths than the gate width required from the specifications of output power because of the requirements of the improved linearity of amplifiers, which is often evaluated by adjacent channel power (ACP). Therefore, an FET which satisfies a high power output as well as a low ACP with a shorter total gate width than conventional FETs' needs to be developed for Digital Cellular Phone Systems.

This paper describes AlGaAs/GaAs power HFETs with uniform characteristics for 0.9 GHz Digital Cellular Phone Systems, which demonstrate a high power density of 117mW/mm and a PAE of 37.6% with a low adjacent channel power (ACP) of -53.4dBc at a low drain bias of 3.3V under 950MHz operating frequency. The power density of the HFET is over 2.5 times as much as that of the conventional MESFET [1].



## Ⅱ. Device fabrication

Figure 1 illustrates a cross-sectional view of HFET based on an AlGaAs/GaAs material system. All

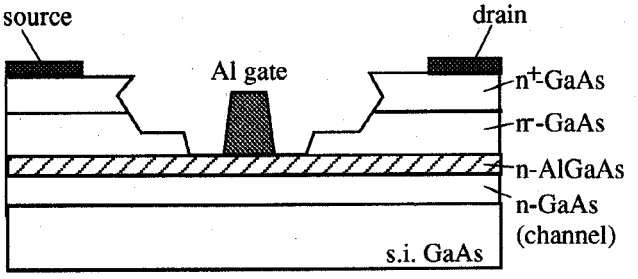


Fig. 1 Cross-sectional view of HFET



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layers were grown on (100)-oriented semi-insulating GaAs substrates by molecular beam epitaxy (MBE). The layer structure is composed of an $n^+$-GaAs cap layer, an $n^-$-GaAs, an n-AlGaAs as a selective etching stopper and an n-GaAs channel layer. This structure leads to higher maximum drain current (Imax) compared with conventional GaAs MESFETs. For the novel HFET, the double recessed gate structure was adopted to suppress the drain current frequency dispersions (gate-lag) [3] and to reduce the source resistance. The recess etching was done by newly-developed wet/dry/wet combined process [3]. The final wet recess etching was selectively stopped on the n-AlGaAs layer. The 0.5μm Al gate was formed by vacuum evaporation and lift-off. This fabrication procedure is very promising for high uniformity device characteristics.

## Ⅲ. Device performance

Figure 2 shows the typical DC I-V characteristics of the HFET. The Imax of 660mA/mm is much higher than that of the conventional GaAs MESFET with the same drain saturation current (Idss). A high transconductance of 240mS/mm and a pinch off voltage of less than 2V have been obtained due to the highly doped GaAs active layer. In spite of this highly doped active layer, a gate-drain breakdown voltage (Vgdo) of more than 10V has been achieved, owing to the optimized double recessed gate structure and doping concentration of n-AlGaAs and $n^-$-GaAs.

A reduced gate-lag time is realized by this double recessed gate structure. Figure 3 (a) and Fig. 3 (b) show the typical drain current (Id) frequency dispersions of the

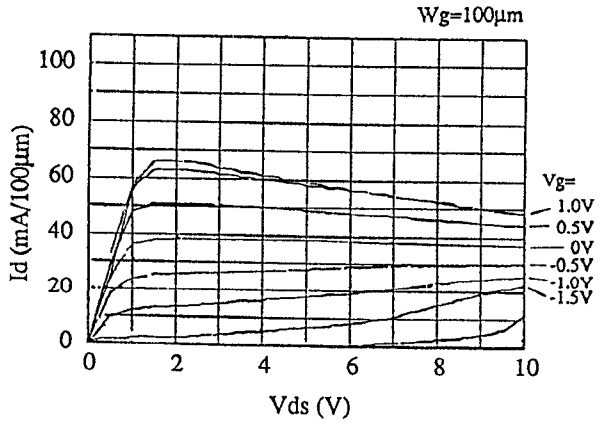
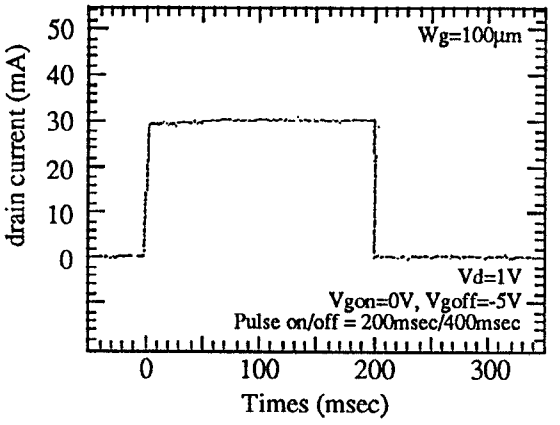
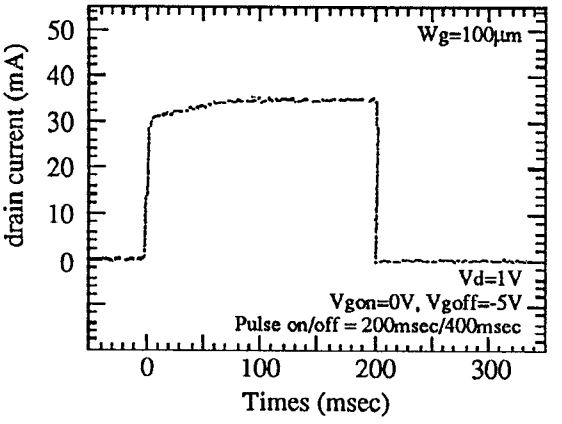



Fig. 2 typical DC I-V characteristics of the HFET




(a)




(b)

Fig. 3 typical drain current frequency dispersions of the double recessed gate HFET (a) and the single recessed gate HFET (b)

double recessed gate HFET and the single recessed gate HFET, respectively. Within 1μsec after the gate pulse signal is applied, Id rises up to over 95% of Idss for the double recessed gate HFET, although 80% for the single recessed gate HFET. These results are due to less influence of the surface depletion layer under the ungated recess region of the double recess structure. Furthermore, a small Idss variation as small as $3\sigma_{Idss}$/Idss of 4.5% in an wafer has been obtained due to the selective chemical etching.

Figure 4 shows the maximum stable and available gain (MSG/MAG) versus frequency. An MSG of 27dB has been obtained at 950MHz.

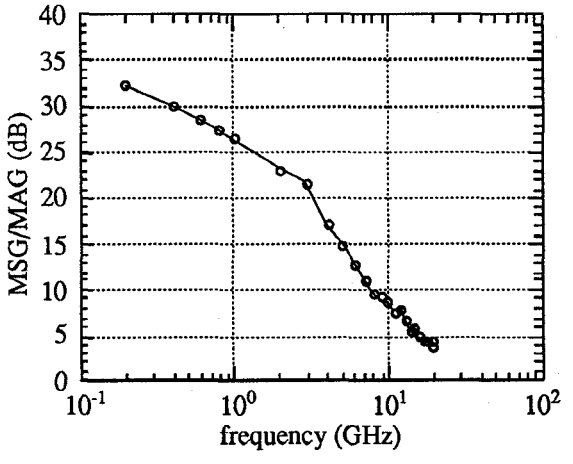



Fig. 4 maximum stable and available gain versus frequency

Figure 5 shows the measured output power and PAE of the device with 2.4mm gate width as a function of input power at a drain bias of 3.3V at 950MHz. The input signal was modulated by π/4-shifted quadrature phase shift keying (QPSK). This device have delivered an output power of 24.5dBm at the 1dB gain compression point with a linear gain of 23.6dB and a PAE of 37.6%. A high power density of 117mW/mm has been successfully attainted.

Figure 6 shows the ACP under the same conditions as Fig. 5. In the figure, L1, U1, L2, and U2 denote the ACP at -50kHz, +50kHz, -100kHz, and

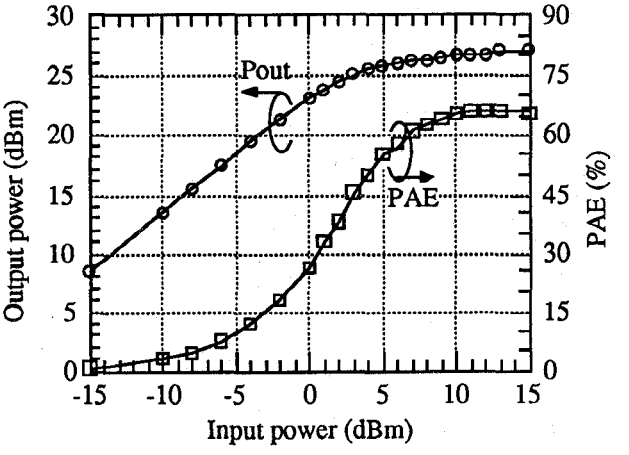



Fig. 5 output power and PAE as a function of input power for the gate width of 300μm x 8 for 950MHz π/4-shifted quadrature phase shift keying modulated input signals

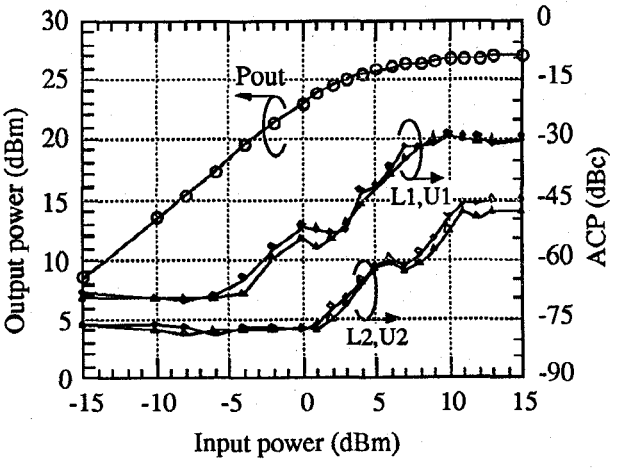



Fig. 6 ACP at ±50kHz and ±100kHz apart from the center frequency of 950MHz under the same conditions as Fig. 5

+100kHz apart from the center frequency of 950MHz, respectively. A low ACP of -53.4dBc has been obtained with a high power density of 117mW/mm. A power amplifier for Digital Cellular Phone Systems is expected to be realized using this HFET with extremely short gate width.

## Ⅳ. Conclusion

We have developed a AlGaAs/GaAs HFET with a high power density for 0.9GHz Digital Cellular Phone Systems. The device have delivered a high power density of 117mW/mm and a PAE of 37.6% with a low ACP of -53.4dBc at a drain bias as low as 3.3V. The novel HFETs are very promising for the improvement of power density and power-added efficiency required for power amplifiers.

## Ⅴ. References

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